Cu-Pillar Bump Probing: Utilizing a 50µm Pitch Fine Pitch Vertical Probe Card Technology

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Outline

- Introduction to Fine Pitch Copper Pillar Bumps
- Testing/Probing Requirements
- Test Vehicle Design
- Probe Card Challenges
- Test Data
- Summary
- Future Work

Introduction

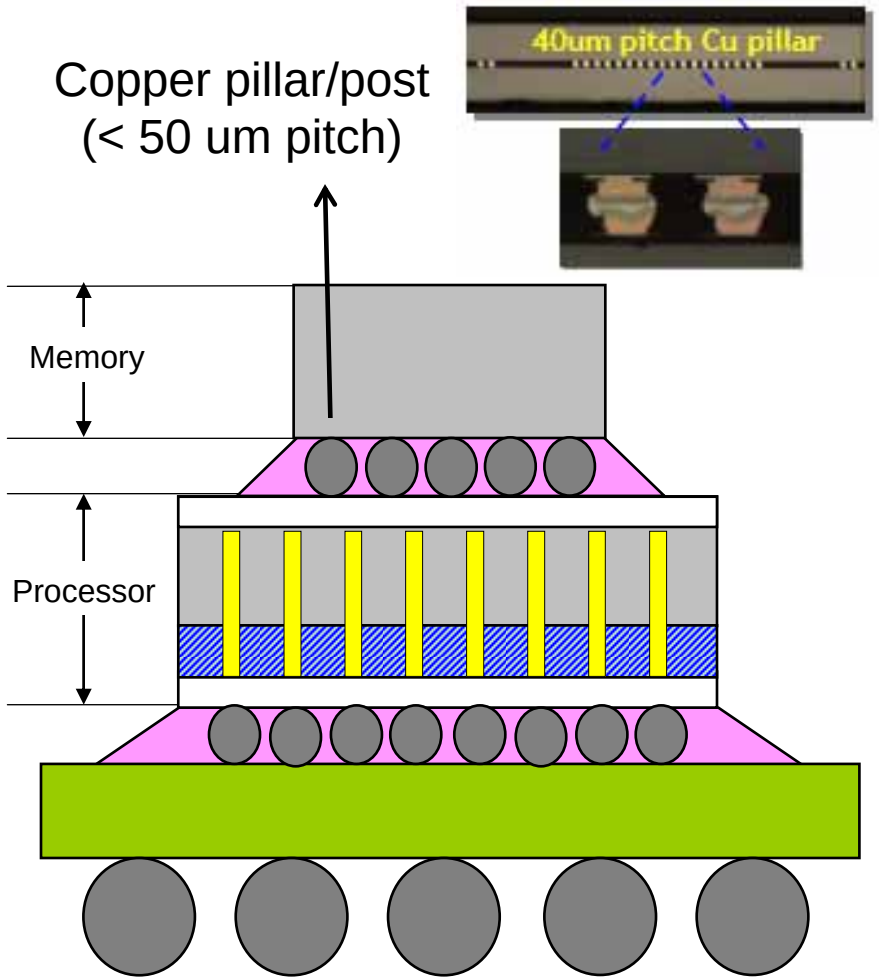
- **Next Generation Flip Chip Interconnects**
  - 2.5, 3D Integration Process
- **Electroplated Copper Pillars with Solder Caps**
- **Advantages**
  - Fine Pitch Capability
  - Increased I/O Density
  - Improved Electrical & Thermal Performance
    - Superior Electro-Migration
  - Higher Reliability at Lower Cost

3D IC Test Challenges

ASE GROUP

- **Wafer Probing**
  - **Thinned wafer handling**
    - Grinding before/after test
    - Assembly flow vs. Test
  - **TSV test**
    - TSV defect
    - Double-sided wafer probing?
  - **Die/wafer contact interface material**
    - Bond pads/ micro bumps/ TSV
    - Cu pillars
  - **Contact force of high I/O number vs wafer thickness**
    - Probe Force
    - Probe material
  - **Fine Pitch**
    - Area array pitch < 50um
    - > 1000 contacts

Fundamental Study Capability Is Required Jointly between Assembly and Test



Testing/Probing challenges

- **Copper Pillar Bump Testing/Probing Challenges**
  - P/C Availability at 50µm & Below in Array Configuration
  - Small Bump Diameter
    - Need Very Low Probing Force
    - Need Very Good Tip Alignment
  - Need Probe Compliance to Accommodate Bump to Bump Variation Across Wafer
  - Bump Material: Lead-free Solder

Goals/Objective

- **Evaluation Objective/Scope**
  - Probe Card Feasibility at 50µm Array
  - Copper Pillar Bump Probing Evaluation
    - Bump Damage Assessment
    - Electrical, Thermal & Mechanical Characterization
    - Post Wafer Probing Tests for Reliability
- **Test Equipment**
  - Test Chip Designed by ASE
  - LT50 Probe Card by SV Probe
  - P-12 XLn Prober, HP93000 Tester
  - Microscope, SEM, Veeco Profilometer

Equipment Utilized

Prober

Tester

Docking

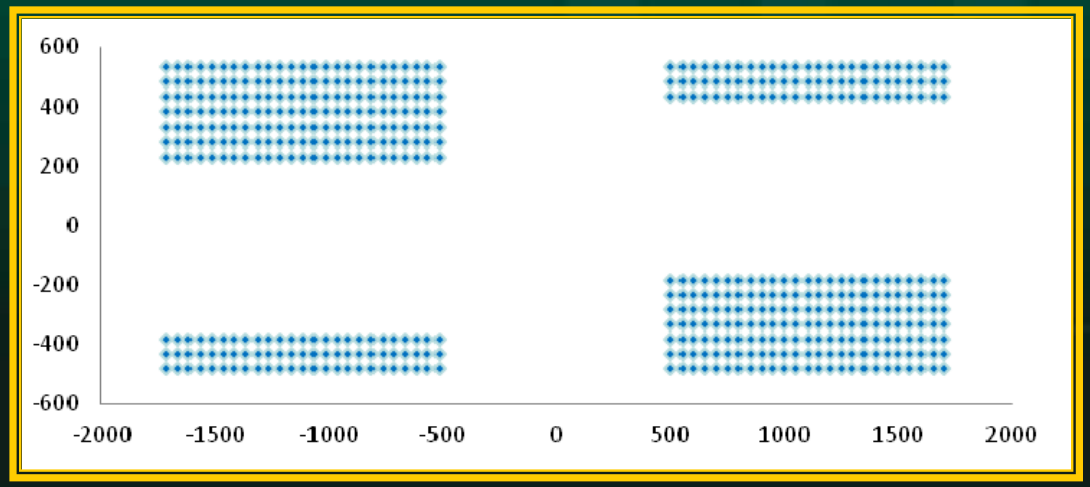
SEM

Veeco

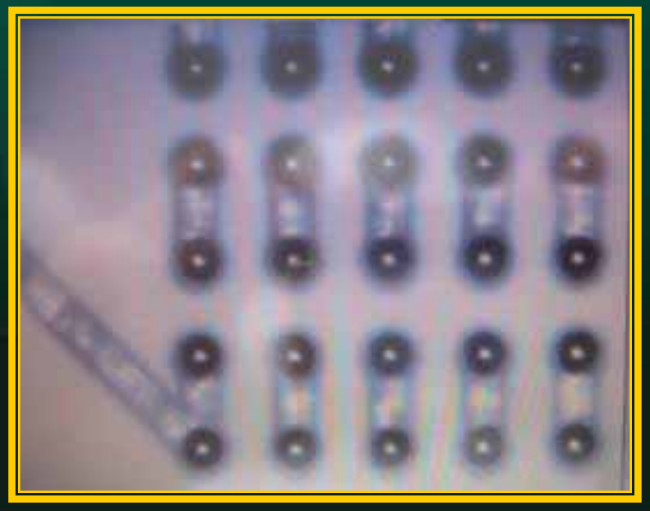
Test Chip Design

- **Test Chip Design Details**
  - 50µm Pitch
  - Array Configuration, 4 Groups, 500 Points Total
  - Daisy-chain Resistance Measurement

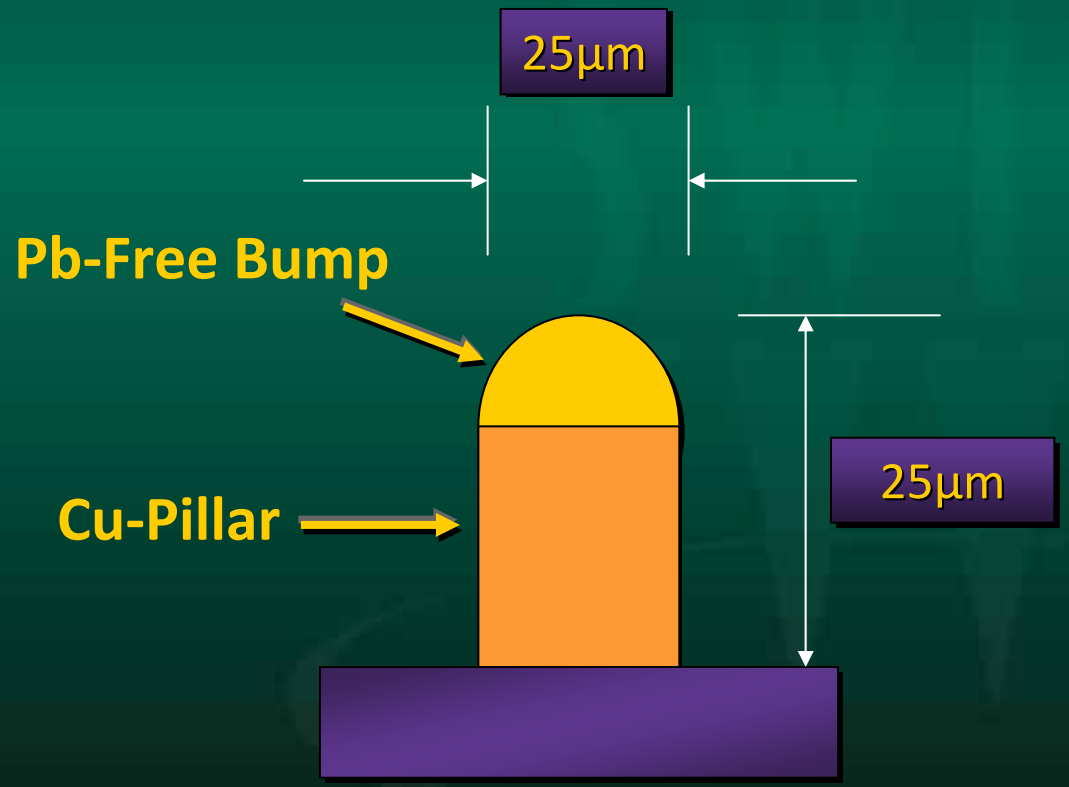
Array Layout



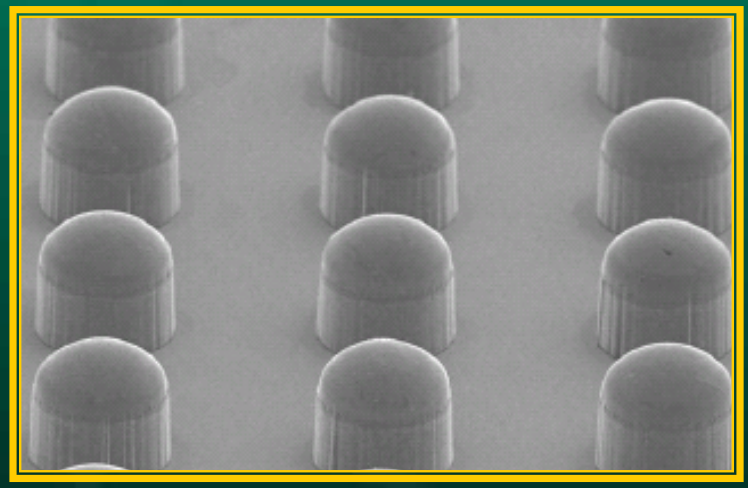
Optical Picture



Cu-Pillar Structure

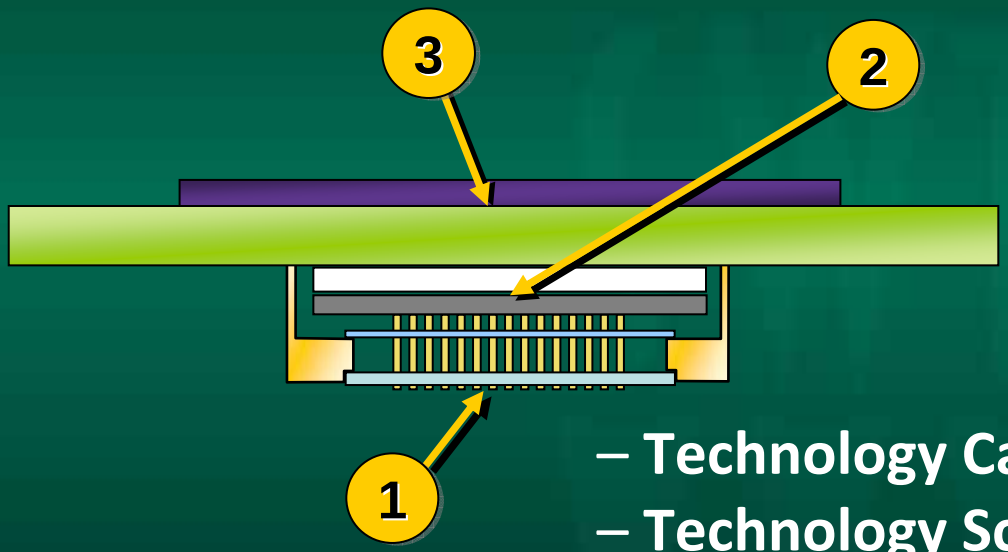


Side View



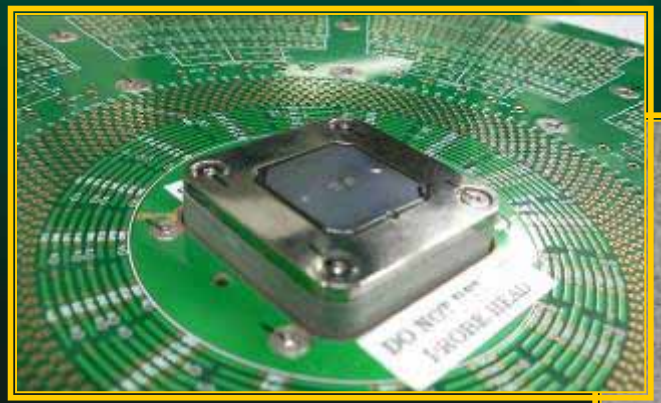
Initial Bump Height : ~25 +/-3µm

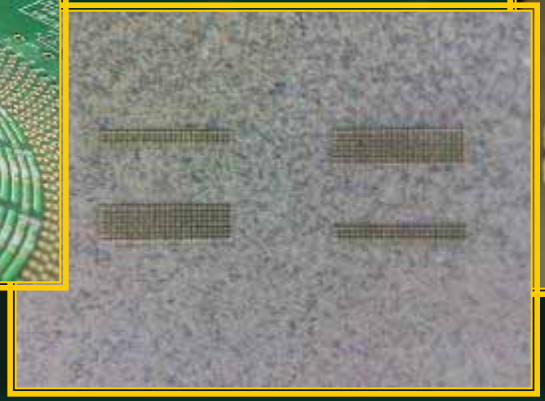
LogicTouch™ Vertical Probing Technology

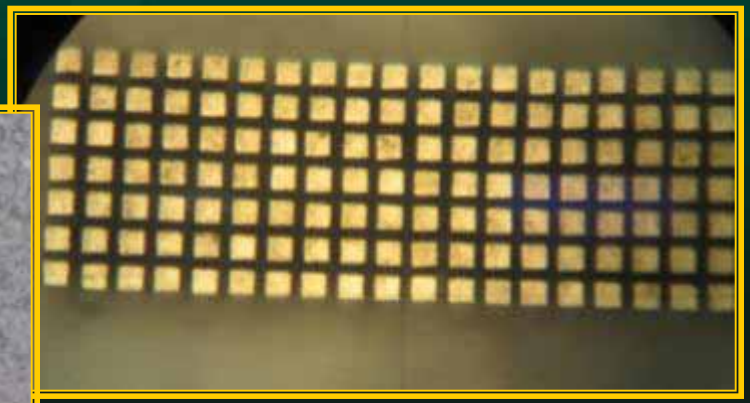


1. Probes
2. Space Transformer (MST)
3. PCB

– Technology Capable of Probing 50µm Arrays
– Technology Scalable to 40µm Pitch



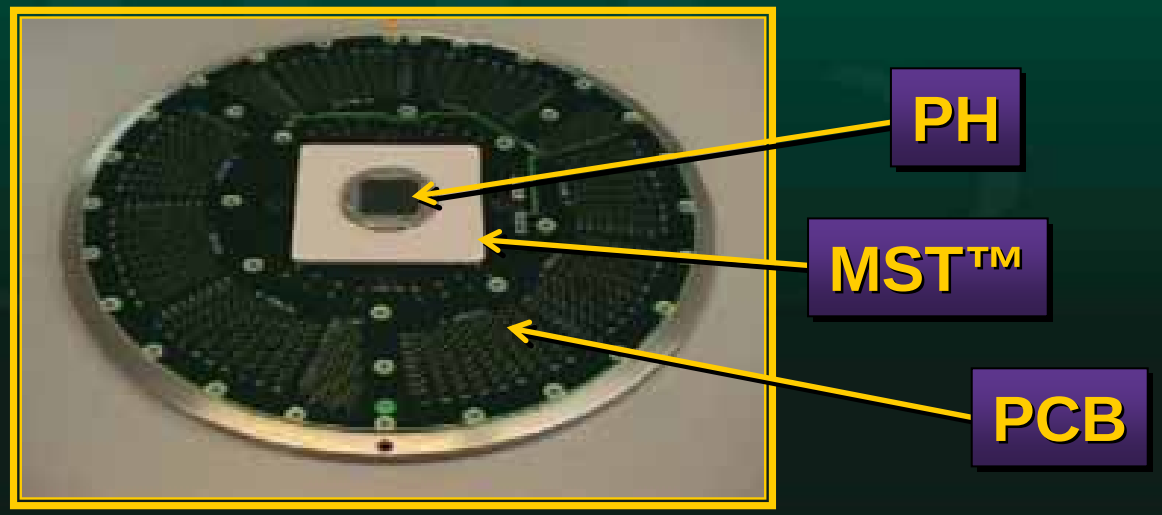




PROBE CARD CHALLENGES

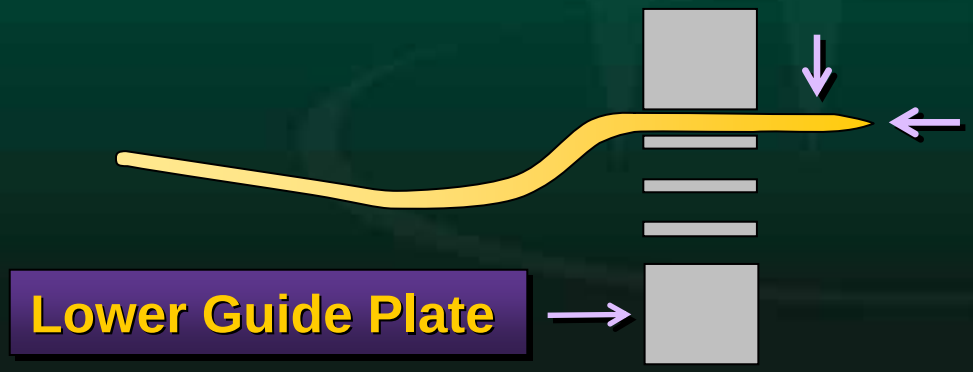
Scalability Challenges

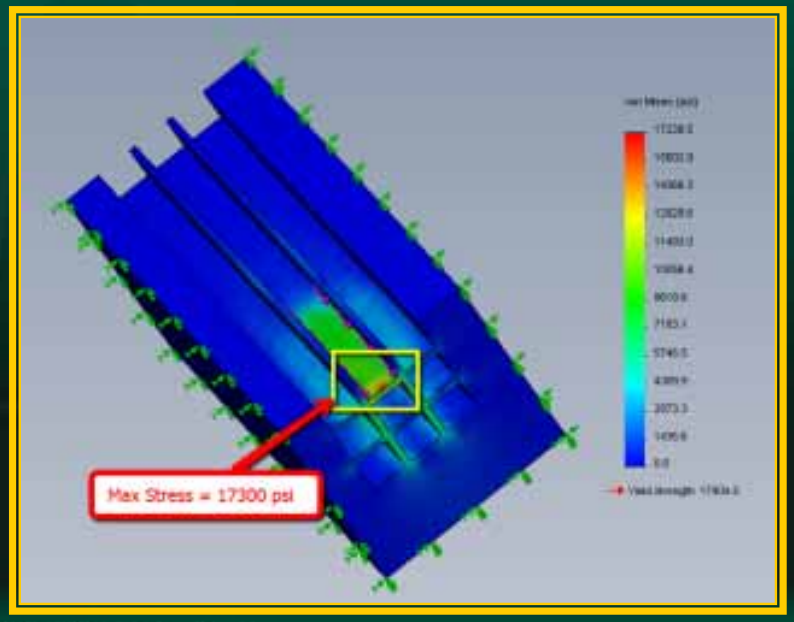
- **Space Transformer Availability at 50µm Pitch Array**
  - Based on Standard Thin Film Technology Capability, Difficult to Achieve Escapement Required for Routing
  - Need Pad on Via at Pitch & Hence MLC/MLO not Feasible for Array Configurations at 50µm Pitch
  - New Type of Interconnect was Developed Internally – the Modular Space Transformer or MST™



Scalability Challenges

- **Guide Plate Wall Strength**
  - Reduced Wall Strength due to Reduced Wall Thickness due to the Spatial Constraints at 50µm Pitch
  - Probes Designed to Minimize Loading on Guide Plate (FEA)
  - Stress/Life Tests at Max OT to Ensure Wall Integrity

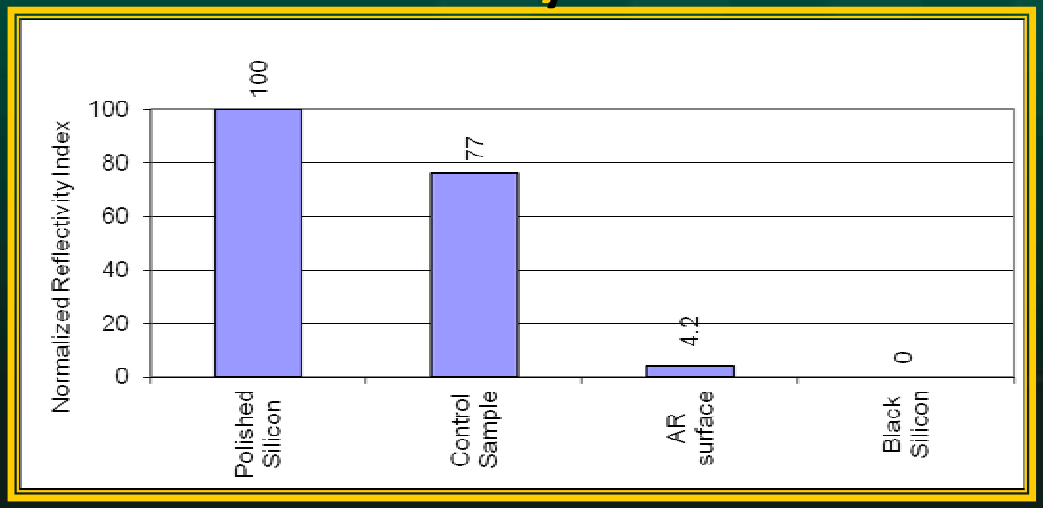




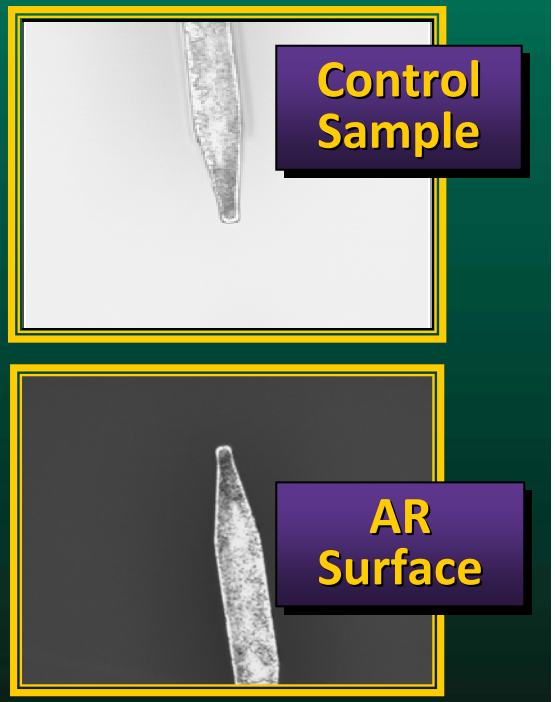
Guide Plate Reflectivity

- **The MEMS Guide-plates Used in LT50 Probe Cards have a Smooth & Polished Surface Finish**
  - Lighting Adjustments may be Required During Probe Card Setup at PCA & Prober
- **Various Anti-reflective Surface Treatments were Evaluated to Reduce Normal Reflection**
  - Surface Scattering (Textured/Engineered Surface)
  - Interference (Thin Films/Coatings)

Veeco Reflectivity Measurement



P-12 Prober

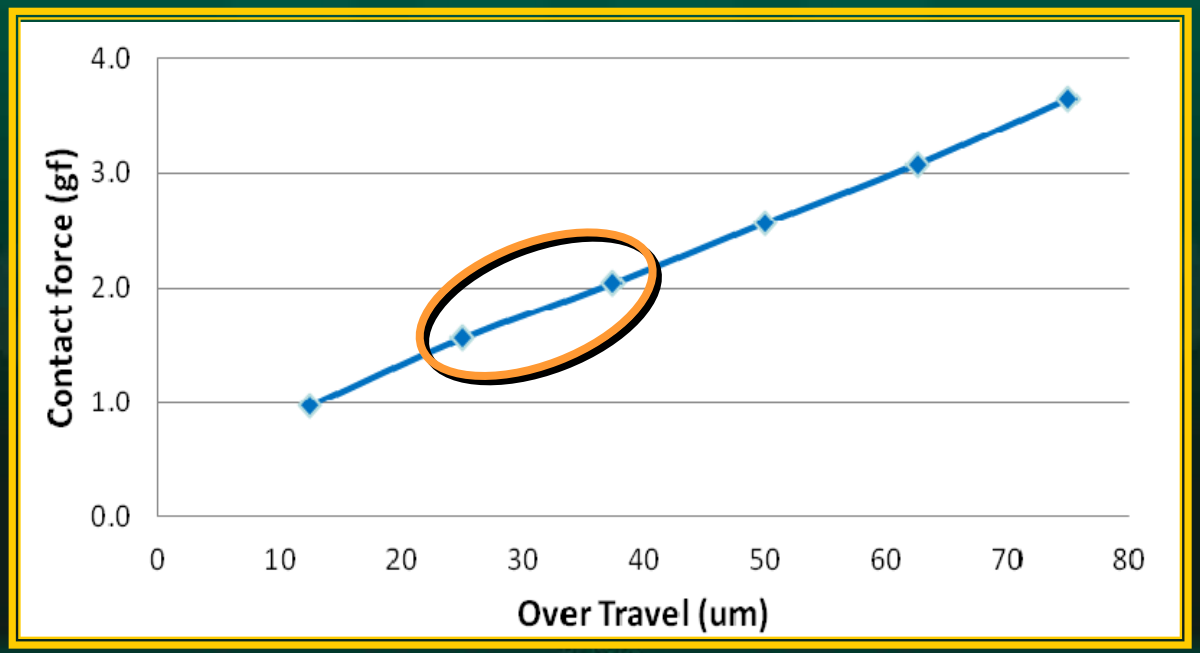


P-12 Prober Pictures: High Mag, Light Level 120, Focused 7-8 mils above Die Surface

PROBE CARD DATA

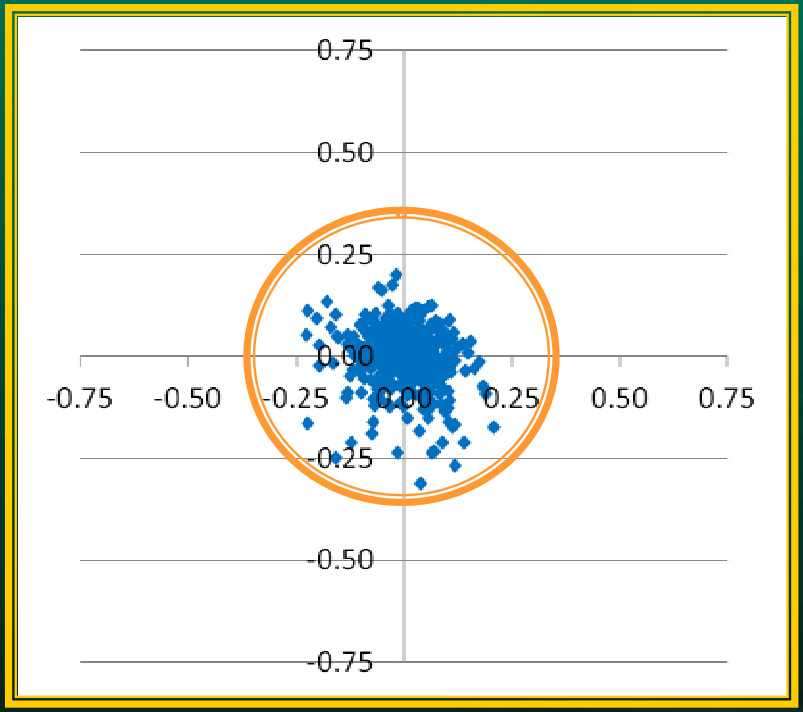
Probe Force

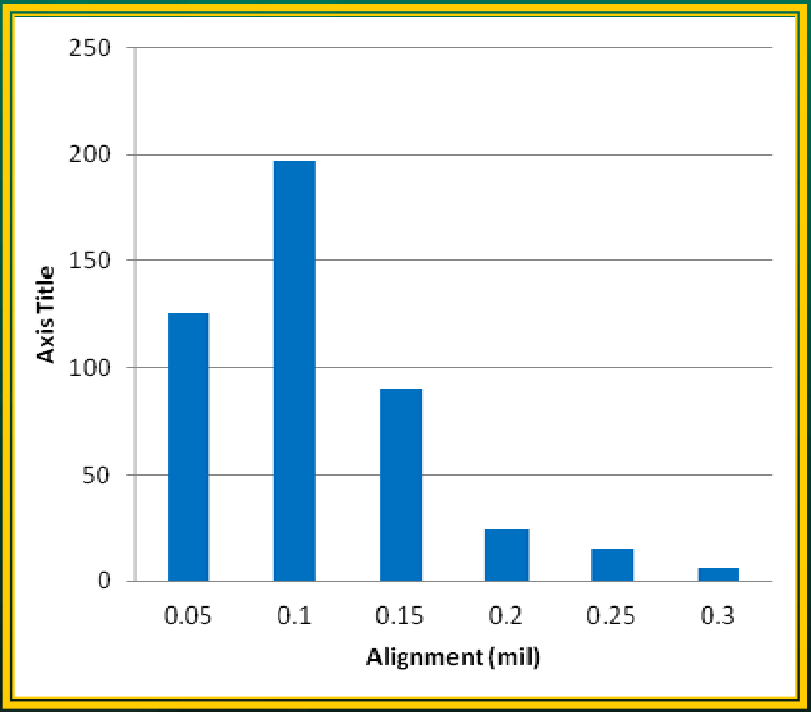
- **Contact Force of 2.5 gf @ 50µm OT**
- **Preferred Bump Probing OT → 25 to 40µm**
  - Minimize Bump Damage
  - Accommodate Bump Co-planarity Across Wafer



Tip Alignment

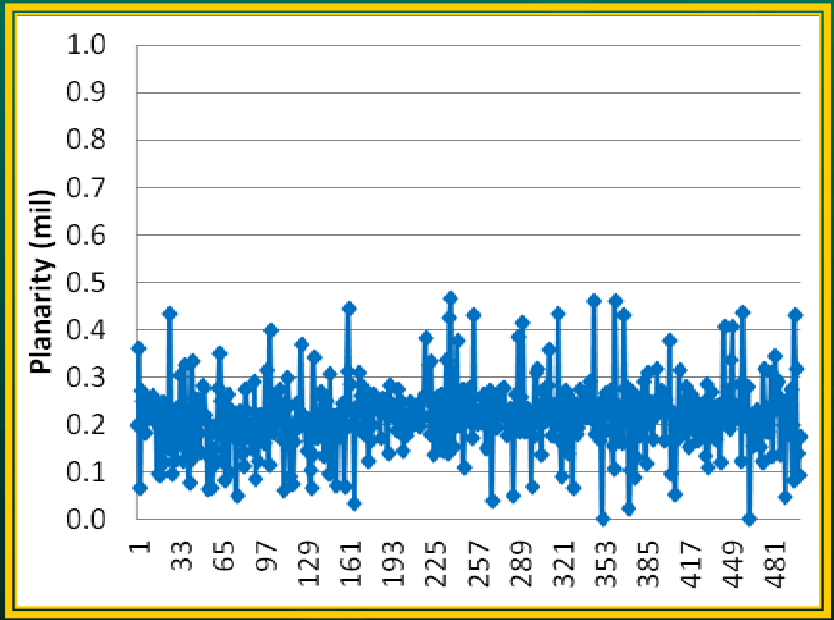
- **Probe Tip Alignment – 0.3 mil Radial**

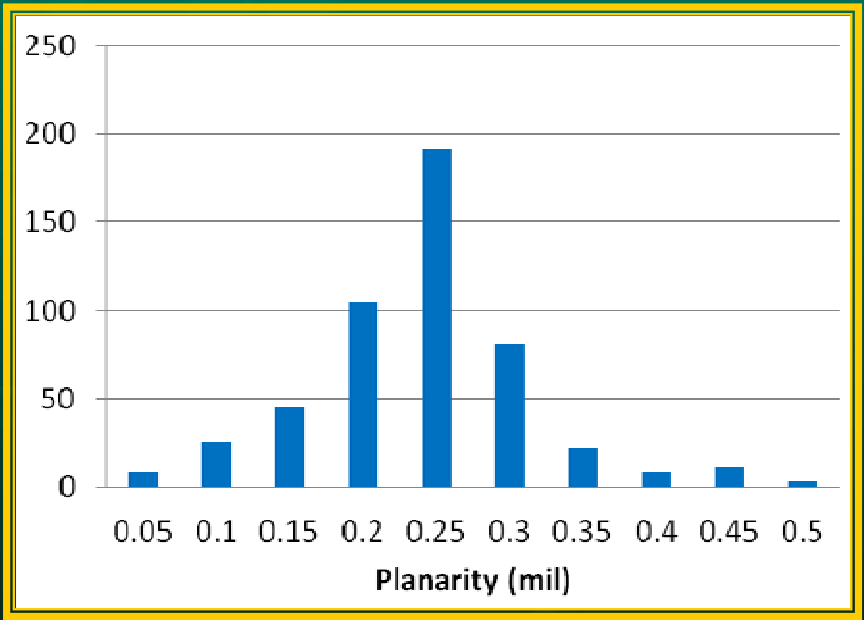




Planarity

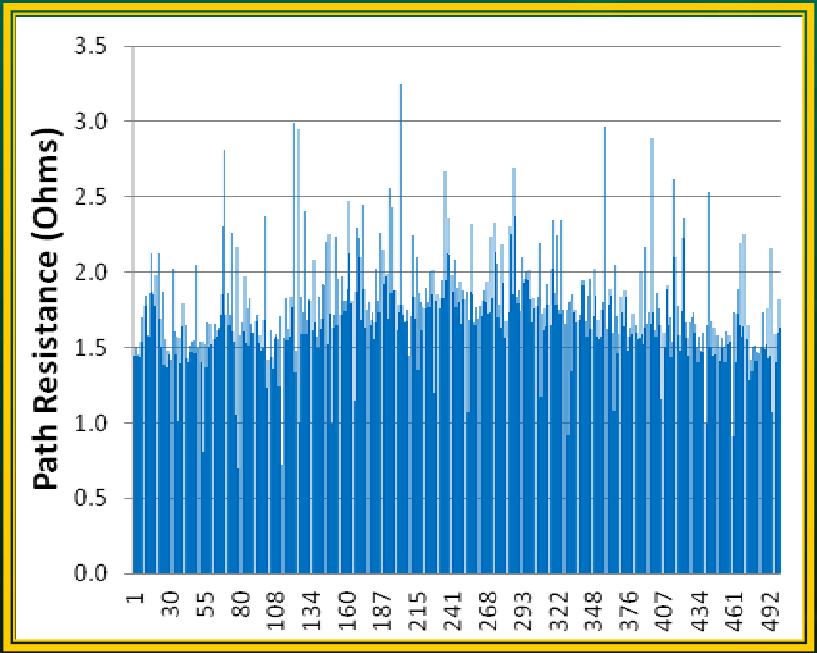
- **Probe Planarity 0.45 mil (12µm)**

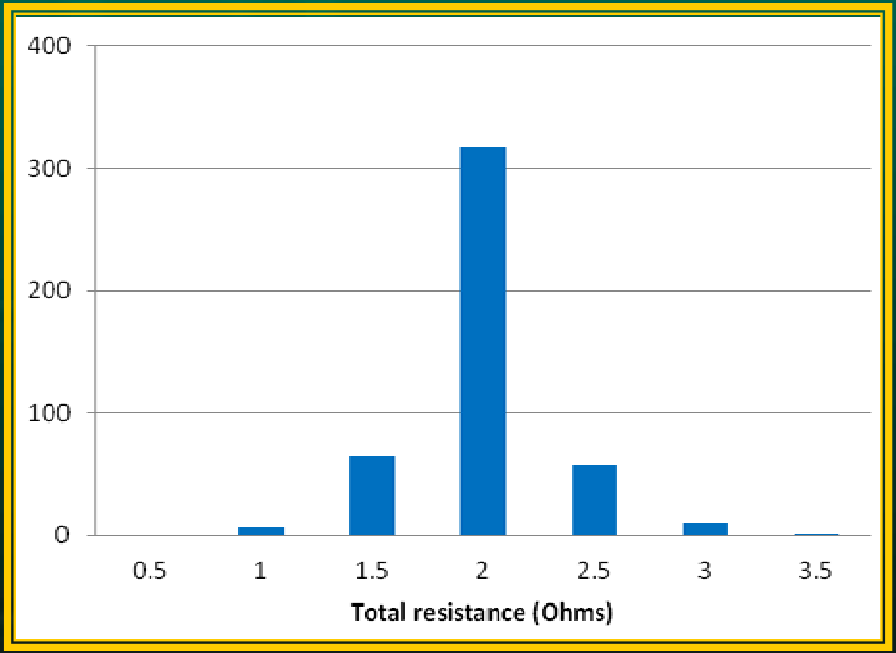




Resistance on Gold

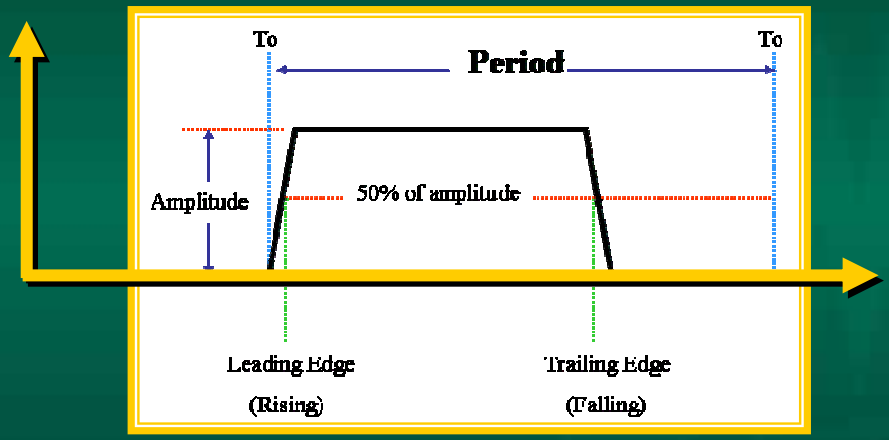
- **Max Total Resistance is 3.2 Ohms (includes Cres & Path Resistance through PH, MST & PCB)**

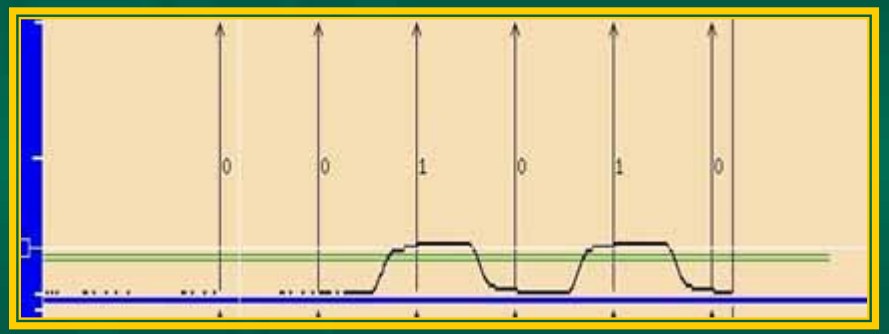


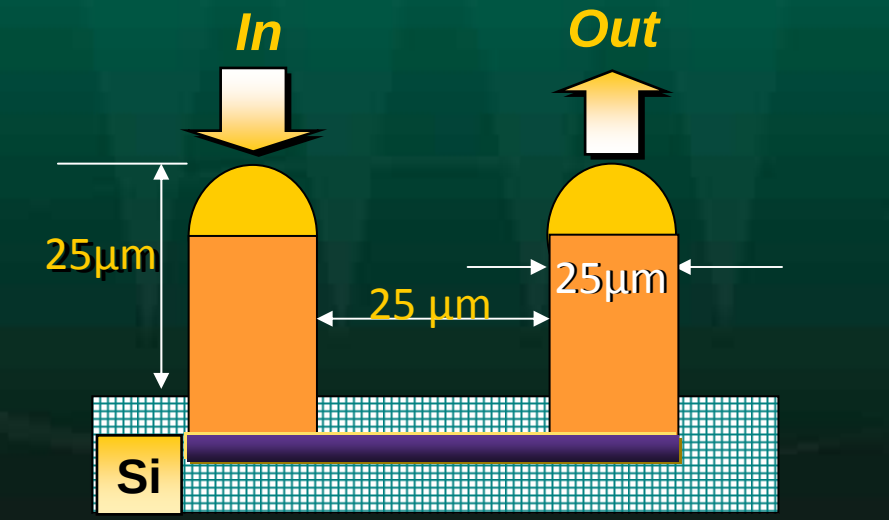


COPPER PILLAR BUMP PROBING

Test Method





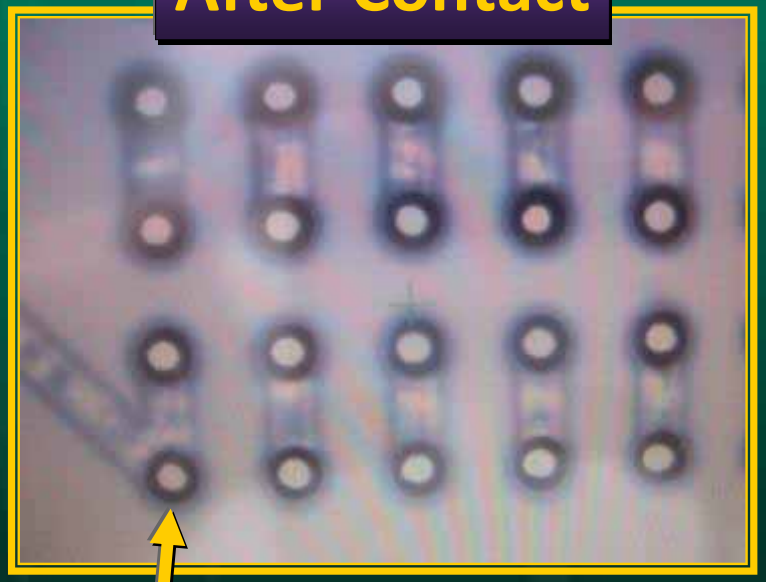


Daisy Chain Bump Structure

Probe Mark

Before Contact

After Contact



Probe Mark Area Under 30%

***Over-Drive: 40µm**

***# probing: 2 TDs**

Tests in Process

- **Electrical Tests**
  - Cres, Leakage Characterization vs. OT, # TD
- **Mechanical**
  - Probe Mark Size Characterization vs. OT, # TD
  - Bump Damage Assessment vs. OT, # TD
- **Thermal**
  - Effect of Temperature (Hot, Room & Cold) on:
    - Probe Card Performance (e.g. Cres Stability, Cleaning etc.)
    - Probe Mark / Bump Damage

Summary / Conclusion

- **To Address Test Challenges Associated with Fine Pitch Copper Pillar Bump Probing**
  - A Test Chip with 25µm Pillar Bumps at 50µm Pitch Array was Designed & Fabricated
  - An LT50 Probe Card at 50µm Pitch Array was Built with SV Probe's Proprietary ST Technology
- **Test / Evaluation**
  - Good Probe Card Tip Alignment & Planarity
  - Max Total Resistance through P/C Including MST was 3.2 Ohms
  - P/C Passed Opens/Shorts Test on Copper Pillar Bumps
  - Probe Mark was < 30% of Bump Area at 40µm OT at 2 TDs
- **Successful Collaboration between ASE & SV Probe & the Preliminary Evaluation Results to Date have been Positive**